CLAIMS

We claim:

 A method for making an electronic-based imaging component, said method comprising the steps of:

providing a processed electronics layer;

providing a photosensing element having an interconnect via, said

photosensing element fabricated in an integrated optically active layer;

said photosensing element substantially decoupled from said

interconnect via;

bonding said optically active layer to said electronics layer, wherein said optically active layer is disposed substantially proximate to a metalization surface of said electronics layer so as to effectively permit fabrication of said interconnect via.

- 2. The method of claim 1, wherein said processed electronics layer is substantially fully processed and said decoupling comprises at least one of physical and mechanical decoupling.
- The method of claim 1, wherein said photosensing element comprises at least one of a photodiode, a photomultiplier, a phototransistor, and a photoconductor.

- 4. The method of claim 1, wherein said optically active layer comprises at least one of Si, GaAs, InP, GaN, HgCdTe, a-Si, p-Si, x-Si, Ge, SiGe, SiC, a monocrystalline material, a polycrystalline material and an amorphous material.
- The method of claim 1, wherein said bonding comprises at least one of wafer-to-wafer bonding and die-to-wafer bonding.
- 6. The method of claim 1, wherein said interconnect comprises at least one metallized via.

7. A method for making an electronic-based imaging component array, said method comprising the steps of:

providing a processed electronics array layer;

- providing a photosensing element array having a plurality of interconnect vias, said photosensing element array fabricated in an integrated optically active layer;
- bonding said optically active layer to said electronics layer, wherein said optically active layer is disposed substantially proximate to a metalization surface of said electronics layer so as to effectively permit fabrication of said plurality of interconnects vias.
- The method of claim 7, wherein the interconnect density comprises about one connection per 10-100 square microns.
- 9. The method of claim 7, wherein said plurality of interconnects comprise a plurality of metallized vias.
- 10. The method of claim 7, wherein the photosensing element fill factor is up to about 75%.
- 11. The method of claim 7, wherein the photosensing element fill factor is greater than 75%.

- **12**. The method of claim **11**, wherein the photosensing element fill factor is up to about 100%.
- 13. The method of claim 7, wherein the CMOS circuitry is optimized for substantial parallel processing of array-captured images.
- **14**. The method of claim **7**, further comprising the step of providing a plurality of vertically integrated optically active layers.
- 15. The method of claim 7, further comprising the step of providing a plurality of vertically integrated CMOS layers.
- 16. The method of claim 7, wherein said optically active layer comprises at least one of Si, GaAs, InP, GaN, HgCdTe, a-Si, p-Si, x-Si, Ge, SiGe, SiC, a monocrystalline material, a polycrystalline material and an amorphous material.

17. A method for making an integrated CMOS-based imaging component, said method comprising the steps of:

providing at least one of a donor SOI wafer and a donor p-type wafer; providing a host CMOS wafer;

optionally at least one of growing and at least partially converting said SOI wafer to p-type;

growing at least one of an intrinsic or p⁻-epitaxial layer on said donor wafer; growing a thermal oxide layer over said at least one of an intrinsic or p⁻-epitaxial layer of said donor wafer;

optionally forming alignment keys in a Si layer of said donor wafer; said alignment keys corresponding to base keys on said host wafer;

defining an optically active, monocrystalline photosensor region in said donor wafer;

fabricating at least one photodiode in said donor wafer using a plurality of ion implant steps;

optionally forming an optically reflective structure over the top surface of said donor wafer;

at least one of planarizing and preparing said donor wafer for bonding; at least one of planarizing and preparing said host wafer for bonding; aligning said host wafer with said donor wafer;

bonding said host wafer with said donor wafer through an interface substantially proximate to metal interconnects of said host CMOS wafer;

- removing substrate material from said donor surface of the resulting donor/host composite structure;
- etching at least one via within at least one region of the donor/host composite structure's top surface down to landing pads of said CMOS wafer; at least one of clearing, metallizing and plugging said vias with a metal; optionally re-planarizing the top surface of said donor/host composite structure;
- optionally forming at least one of a top side anti-reflective coating and a top side passivation layer; and

opening access vias to I/O pads embedded in said CMOS wafer.

- 18. The method of claim 17, wherein said optically active photosensor region comprises at least one of Si, GaAs, InP, GaN, HgCdTe, a-Si, p-Si, x-Si, Ge, SiGe, SiC, a monocrystalline material, a polycrystalline material and an amorphous material.
- 19. The method of claim 17, wherein said host CMOS layer is substantially fully pre-processed.
- 20. The method of claim 17, wherein said bonding of said host wafer with said donor wafer comprises at least one of wafer-to-wafer bonding and die-to-wafer bonding.